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THICK THERMAL OXIDE LAYERS AND ISOLATION REGIONS IN A SILICON-CONTAINING SUBSTRATE FOR HIGH VOLTAGE APPLICATIONS

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[0001] # THICK THERMAL OXIDE LAYERS AND ISOLATION REGIONS IN A SILICON-CONTAINING SUBSTRATE FOR HIGH VOLTAGE APPLICATIONS

[0002] 1. Field of the Invention

[0003] In general, the present invention relates to a method creating thick thermal oxide layers on silicon. Also, the present invention relates to a method of separating high voltage areas within a silicon chip, wafer, or stack of silicon chips, or stack of silicon wafers. The present invention also relates to a method of integrating and connecting vertical feedthroughs in a stack of silicon layers.

[0004] 2. Brief Description of the Background Art

[0005] Various processes have been developed to create isolation regions in silicon. One of the popular methods of creating isolation regions within a silicon substrate is through thermal oxidation of areas of silicon itself. For example, in U.S. patent No. 5,410,176 to Liou et al., issued April 25, 1995, the inventors describe a method for forming isolation structures in an integrated circuit. First step is masking all the active regions on the silicon. After masking recesses are etched into the exposed silicon to a depth on the order of the final thickness of the insulating isolation structure. Sidewall spacers of silicon dioxide, or another insulating amorphous material are disposed along the side walls of the recess, with silicon at the bottom of the recesses exposed. Selective epitaxial growth of silicon is then used to form a layer of silicon within the recesses, preferably to a thickness on the order of half of the depth of the recess. The epitaxial silicon is thermally oxidized, filling the recesses with thermal silicon dioxide, having a top surface which is substantially coplanar with the active regions of the surface.

[0006] In U.S. Patent No. 5,863,826 to Wu et al., issued January 26, 1999, the inventors disclose a method for forming field isolation regions in multilayer semiconductor devices comprising the steps of masking active regions of the substrate, forming porous silicon in the exposed field isolation regions, removing the mask, and oxidizing the substrate. A light ion impurity implant is used to create pores in the substrate. Substrate oxidation proceeds by rapid thermal annealing because the increased surface area of the pores and the high reactivity of unsaturated bonds on these surfaces provides for enhanced oxidation.

[0007] In U.S. Patent No. 5,189,501 to Kawamura et al., issued February 23, 1993, the inventors describe an isolator for isolating semiconductor devices, components of an integrated circuit, on a semiconductor substrate, wherein the isolator is delimited by walls of a trench formed on a top surface of the semiconductor substrate, where the trench filled with a silicon oxide layer deposited by a chemical vapor deposition method. A small ditch created in the middle of a top surface of the silicon oxide layer in the trench is filled with silicon, and at least a top surface of the silicon is thermally oxidized to form another silicon oxide layer.

[0008] In U.S. Patent No. 5,386,142 to Kurtz et al., issued January 31, 1995, the inventors describe a semiconductor structure having environmentally isolated circuit elements disposed thereon. The semiconductor structure has a first semiconductor wafer having a semiconductor element such as a piezoresistive element or any integrated circuit located on a top surface thereof. The first wafer is bonded to a second semiconductor wafer so that the semiconductor element on the first wafer is received in a cavity sealed from the outside environment. The bottom surface of the second wafer is prepared by etching it about a mask pattern so that the pattern projects from the bottom surface,

thereby forming a cavity and defining projecting surfaces which are bonded to corresponding projecting areas on the first wafer to create a hermetic seal there between. The second wafer is electrochemically etched to produce porous silicon with regions of non-porous monocrystalline silicon extending between the top and bottom surfaces. The porous areas are thermally oxidized to convert them to silicon dioxide while the non-porous regions bonded to bond pads of the resistive pattern on the first wafer act as extended contacts.

[0009] Applicants' review of the background art in general has indicated that in order to handle high voltages the silicon oxide layer needs to be thick. Two micron of silicon oxide layer thickness is needed to handle a voltage of about 1 kV. In order to handle a voltage of 3-5 kV, the silicon oxide layer thickness should be in the range of 6-10 μm. Generally a thickness of 3 μm silicon oxide layers can be formed by long wet thermal oxidation. However 3 μm thickness is not sufficient to handle a voltage of 3-5 kV reliably since pinholes and other artefacts in the oxide can lower the breakdown voltage.

[0010] In the field of semiconductor device fabrication, particularly with the continuing trend toward smaller device feature sizes, micromachining technology compatible with semiconductor processing is a necessity. Microcolumns which are miniaturized electron optic devices facilitate smaller device fabrication. Generally, microcolumns are made of pyrex and silicon. But, pyrex can not be machined with as high a precision as silicon. Therefore, it would be advantageous to find a method enabling fabrication of microcolumns out of silicon alone. However to handle high voltages, portions of the silicon need to be converted to silicon oxide which has a thickness in the range of 6-10 μm. As stated above, with the general methods available

today a silicon oxide thickness which can be generated within a reasonable time by wet thermal oxidation is about 3μm (which is generated in about approximately 18 hours at a temperature of 1100° C).

[0011] Often, isolation regions are created within silicon structures for various purposes, for example, to often protect circuit elements within one region from interfering with the functions of circuit elements in another region. Some of these isolation regions need to provide insulation from high voltages. In order to accomplish high voltage insulation, it would be useful to be able to partition silicon structures with thick silicon oxide layers having a thickness in the range of about 2 μm/kV of applied voltage.

[0012] Therefore, there is a need to create thick silicon oxide layers within as on the surfaces of silicon structures. For many semiconductor devices, thickness ranging from greater than 3 up to about 10 μm are particularly useful.

SUMMARY OF THE INVENTION

[0013]

[0014] One of the embodiments of the invention involves a method of forming a thick silicon oxide layer upon or internal to a silicon structure. This embodiment includes a step of etching a plurality of trenches in or openings through a silicon structure. For example, the etching may be conducted by deep dry silicon etching. With respect to the of the plurality of trenches each trench is separated from an adjacent trench by a trench wall. The silicon is then oxidized. During oxidation the silicon expands. Normally, 1 micrometer of silicon is converted to about 2 μm of silicon oxide. In other words, during the oxidation process a lateral expansion takes place. The invention takes

advantage of this phenomenon. By appropriately selecting the thickness of the walls between trenches and the trench opening width, each trench can be entirely filled with silicon oxide by oxidizing the trench walls. The number of trenches required to oxidize a large area is based on time considerations since the oxidation process is a diffusion limited process. The depth of an oxide layer on a silicon structure surface can be determined by fixing the depth of the trenches (the height of the trench walls). The trench walls will be consumed to form a layer of silicon oxide at the surface of the silicon. Deeper trenches can be etched by increasing the aspect ratio during the etch process.

[0015] Another embodiment of the invention, pertains to a method of creating isolation regions within a silicon structure, which isolation regions can withstand high voltages. This embodiment involves etching of a trench or opening of desired shape or shapes into the silicon structure creating an opened shaped portion. If a shape is etched completely through the silicon structure then the shaped portion may be severed from the silicon and drop out. In order to prevent the shaped portion from dropping out, bridges of silicon are maintained across a through-opening at nominal distances during the etching process. The exposed silicon surfaces and the silicon bridges are oxidized. The oxidation causes the silicon to expand, enabling filling of an open space with an oxide layer. The oxide layer separates the shaped portion from the rest of the silicon structure, thus creating a shaped region isolated from the rest of the silicon structure. During the oxidation process, the silicon oxide layer is formed not only in the trenches but also on the surfaces of the silicon. The oxide layer can be etched and removed from areas where it is not desired. Isolation regions of various shapes and sizes can be created using this method.

[0016] The present invention also relates to a method of integrating and connecting vertical feedthroughs and of providing vertical interconnects in a stack of silicon structures. This embodiment involves at least two silicon structures. The two structures could be silicon layers within a silicon chip or a wafer, or a stack of silicon chips, or stacks of wafers. Isolation regions can be generated within the silicon structures using the methods described above. Electrical and/or mechanical connections are established through the semiconductor regions in each of the structures. These isolated semiconductor regions can act as feedthroughs for electrical connections which connect different layers within a silicon chip or wafer. Mechanical and electrical connections of stacked chips or wafers can be achieved through fusion bonding, anodic bonding or eutectic processing, for example, but not by way of limitation.

[0017] Yet another embodiment of the invention involves a method of creating semiconductor regions of various shapes separated by oxide layers or oxide layers in combination with vacuum which is an excellent insulator. This embodiment involves etching a trench or opening of desired shape or shapes into the silicon structure creating a shaped portion. If a shape is etched completely through the silicon structure, then the shaped portion may be severed from the silicon and drop out. In order to prevent a shaped portion from dropping out, bridges of silicon are maintained across the trench. These bridges give support to the shaped portion. The exposed regions are then oxidized. Once again, the silicon oxide formed expands and fills a portion of the opening or trench. A space is left between the silicon oxide layer covering the shaped portion and the silicon oxide layer covering the surface of the remainder of the silicon structure. A vacuum may be maintained in the space separating two of the oxide layers to provide improved electrical insulation.

[0018] **BRIEF DESCRIPTION OF THE DRAWINGS**

[0019] Figures 1A through 1D are cross-sectional schematics of a silicon structure showing a series of steps which create a silicon oxide layer on a silicon structure.

[0020] Figure 1A shows a schematic of a cross section of a silicon structure 101.

[0021] Figure 1B shows the Figure 1A schematic structure after trenches have been etched on its surface.

[0022] Figure 1C shows the Figure 1B schematic structure after the exposed surfaces have been oxidized.

[0023] Figures 2A-2D show schematics of a series of method steps which create a silicon isolation region in a silicon structure.

[0024] Figure 2A shows a schematic of top view of a silicon structure, 200.

[0025] Figure 2B shows the schematic top view of Figure 2A after through-openings have been etched through silicon structure 200.

[0026] Figure 2C shows the schematic top view of figure 2Bafter exposed surfaces of the structure have been oxidized.

[0027] Figure 2D shows the top view schematic of Figure 2C after the oxide layer has been removed from the top and bottom surfaces of silicon structure 200.

[0028] Figures 3A through 3C show another embodiment of the invention where a series of method steps provide electrical isolation in a silicon substrate.

[0029] Figure 3A a shows a cross-sectional schematic of two silicon structures each having electrical isolation regions.

[0030] Figure 3B shows the Figure 3A schematic after the two silicon structures has been bonded to create a structure 350.

[0031] Figure 3C shows the Figure 3B schematic structure 350 after an opening has been formed into the silicon structure, where the opening is available to act as a feedthrough.

[0032] Figures 4A through 4C show an embodiment of the invention where a series of method steps provide electrical isolation of a conductive center region from an exterior structure.

[0033] Figure 4A shows a schematic of a silicon structure, 400 having a cylindrical shape etched partially through it from each side, with an unetched area in the center.

[0034] Figure 4B shows the Figure 4A schematic after the exposed surfaces of the silicon structure has been oxidized..

[0035] Figure 4 C shows the Figure 4B schematic after removal of oxide from the top and bottom surfaces of the structure.

[0036] Figure 5A through 5C shows another embodiment of the invention where a series of method steps provide electrical isolation of a conductive center region from an exterior structure.

[0037] Figure 5A shows the schematic of a silicon structure, having a cylindrical shape etched through it, with spokes connecting the conductive or semiconductive center region to the conductive or semiconductive exterior structure.

[0038] Figure 5B shows the Figure 5A schematic after oxidation of exposed surfaces.

[0039] Figure 5C shows the Figure 5B schematic after the removal of oxide from the top and bottom surfaces of the structure.

[0040] **DETAILED DESCRIPTION OF THE INVENTION**

[0041] As preface to the detailed description, it should be noted that, as used in this specification and the appended claims, the singular forms "a", "an", and "the"

include plural referents, unless the context clearly dictates otherwise.

[0042] As described above, the present invention pertains to a method of forming thick silicon oxide layers on or inside a silicon-containing structure. Also, the present invention pertains to a method of creating isolation regions within silicon which can withstand high voltages.

[0043] Figure 1A shows a cross sectional schematic of silicon 101 starting structure, 100. Figure 1B shows the same silicon structure 100 after the etching of trenches 102 into the silicon 101. The trenches 102 are separated by a trench wall 104 which exhibits a height, h,108, and a trench opening width, w, 106. The trenches can be etched by providing a masking pattern on the surface of the silicon structure 100, using techniques known in the art, and then conducting plasma etching or wet etching of the silicon through the mask using known etch techniques. Known plasma etching techniques enable the etching deep trenches having an aspect ratio as high as 50 : 1. If the trench is to be entirely filled with silicon oxide, the trench opening width 106 of trench 102 should be two times the trench wall thickness 105 of wall 104.

[0044] Figure 1C shows the same silicon structure 100 after oxidation of the surfaces of Figure 1B. A silicon oxide layer 112 has formed on the upper surface 103 of silicon structure 100. A thin silicon oxide layer 113 forms on other exposed surfaces as well. The trench opening width may be such that the entire trench will not be filled during the oxidation, if it is desired to form conduits between isolation areas. The trench wall thickness 105 of trench walls 104 is limited by the time available for carrying out the oxidation process. Typically the oxidation is thermal oxidation, as this provides a non-contaminated oxide. In the case of a typical wet thermal oxide formation, at 1100° C, a 2 micrometer wall thickness requires about 8 hours for conversion to 4 micrometers

of silicon oxide, by way of example and not by way of limitation.

[0045] Patterning of the silicon structure prior to oxidation is carried out so that thick oxide layers are formed only at intended surfaces. By this process it is possible to obtain a thick oxide layer, which is about 20 to 50 times thicker than what is possible using other fabrication methods. Unwanted thin oxide layers may be removed from desired surfaces by masking surfaces which are not to be etched, and dipping the structure in 10% buffered hydrofluoric acid solution.

[0046] The mechanical stress caused by the formation of thermal oxide depends on the patterned structure, the thickness of walls converted to oxide and other factors. The mechanical stress thus created can be released using a variety of techniques. Some of the suggested examples are stress release structures built into the silicon structure itself. Double sided structuring of a wafer is another means to compensate for the mechanical stress caused across the wafer by the thermal oxide formation. By oxidizing both sides of a wafer the stress created on one side may be balanced by the stress on the other side.

[0047] Figure 2A, shows another embodiment of the invention which may be used to provide electrical isolation in a silicon substrate. Figure 2A shows a schematic of top view of silicon structure 200. This embodiment of the invention involves a method of creating isolation regions within the structure 200. Figure 2B shows a schematic top view of the Figure 2A after openings 206 have been etched all the way through the silicon structure, 200 at nominal distance apart. Openings 206 are separated by walls, 208. The openings 206 have a width w_1 represented by the numeral 212 and walls 208 have a thickness t_1 represented by the numeral 214.

[0048] Figure 2 C, shows the Figure 2B structure after the exposed surface of the

silicon is oxidized. Silicon oxide layers are formed during the oxidation. A thin silicon oxide layer 230 covers the entire silicon structure 200. A thick silicon oxide layer 238 forms through the area which was etched to form openings 206, creating two electrically isolated silicon regions 232, and 234. During oxidation, the walls 208 are oxidized and expand laterally to form one continuous silicon oxide layer 238. Figure 2 D shows the schematic top view of the Figure 2C structure after oxide layer 230 is removed from at least upper surface 239 and lower surface 240 of processed structure 200. These surfaces 239 and 240 are typically lapped and polished to provide access to the underlying silicon. The silicon oxide layer 230 may be removed from all sides if desired. The thick silicon oxide layer 238, separates the two electrically isolated silicon regions 232 and 234. Patterning of the silicon structure prior to oxidation is carried out in a manner such that the thick oxide layers form only on intended surfaces. Various anodisation processes as well as thermal oxidation may be used to grow thick oxide layers.

[0049] Another embodiment of the invention pertains to a method of integrating and connecting vertical feedthroughs and providing vertical interconnects in a stack of silicon structures. Figures 3A-3C illustrate the various steps involved in such a method. Figure 3 A shows a schematic side view of two silicon structures 302 and 304, which are bonded together during device fabrication. Both ends of the silicon structures 302 and 304 are covered by thin silicon oxide layers 301 and 319 respectively. Structure 302 contains semiconductor regions 314, 315 and 316. Adjoining semiconductor regions 314 and 315 are separated by a silicon oxide region 308, which acts as an electrical isolation region. The semiconductor region, 315 is also bounded by silicon oxide isolation layers, 306a on the top and 306b on the bottom. Structure 304 contains semiconductor regions 318, 320, and 322. Semiconductor regions 318 and 320 are separated from one another

by a silicon oxide electrical isolation layer 310. The semiconductor regions 320 and 322 are separated from one another by a silicon oxide electrical isolation layer 312.

[0050] Figure 3 B shows the structures of Figure 3A after bonding. Here the semiconductor regions 314 and 318 are combined to form the semiconductor region 330. The regions 315, 316 and 322 are combined to form the semiconductor region 334. The region 320 remains in electrical isolation from the other semiconductor regions by the silicon oxide layers 308/310 306b, and 312. The two structures can be bonded through various processes, for example, fusion bonding, or eutectic processing. With reference to Figure 3A, the thick oxide layers 306a and 306b on the surfaces of the structure 302 are created using the method described in Figures 1A through 1D. The thick oxide layer 308 through structure 302, and the thick oxide layers 310 and 312 through structure 304 are created using the method described with reference to Figures 2A, through 2D. The structures 302, and 304 could be two layers within a silicon chip, could be two wafers or could be present within a stack of silicon chips or stacks of wafers.

The two structures 302 and 304 are bonded together using methods described above. The structures 302 and 304 are aligned and bonded together as shown in Figure 3B, establishing connections between semiconductor regions 314 and 318, and also between semiconductor regions 316 and 322. The bonded semiconductor regions act as interconnects which are electrically isolated by bonded thick silicon oxide layers 308/310 and 306b/312. The bonded semiconductor regions 314, and 318 may be used as an electrical connector to a chip carrier. As can be seen in Figure 3B, the bonded structure will provide a high voltage isolation between the areas 314/318, 320 and 315/316/322.

[0051] Figure 3 C shows the Figure 3B structure after an opening 338 is formed vertically through the thick oxide layer 332. The opening 338, created through the

silicon oxide layer 332, acts as a vertical feedthrough for a conductive interconnect (not shown). The opening 338 can be used to feed wires or other connectors to other structures (not shown). In one embodiment, a metal coating could be deposited inside opening, 338.

[0052] Conductive or semiconductive structures electrically isolated by isolation regions of different shapes can be made using the above described techniques. A semiconductive structure can be made more conductive by the addition of dopants where required.

[0053] Figures 4A, through 4C illustrate, by way of example, the generation of a cylindrical isolation region through a silicon structure 400, where a conductive or semiconductive cylindricall region, 406 is isolated from a surrounding conductive or semiconductive region 404 by a thick oxide layer. Silicon structure 400 includes a front surface 401a, a back surface 401c, a first side surface 401b, a second side surface 401d, a top surface 401e, and a bottom surface 401f. A cylindrical through-opening 402 is etched through the silicon structure 400. The cylindrical through-opening 402 separates the conductive cylindrical region 406 from the surrounding conductive region 404. To maintain conductive cylindrical region 406 in place in structure 400 during processing, the through-opening 402 is etched partway through structure 400 from top surface 401e and partway through from the bottom surface 401f, leaving a disk of silicon 408 of nominal thickness bridging conductive cylindrical region 406 to the surrounding conductive region 404.

[0054] Figure 4B shows the Figure 4A structure after thermal oxidation. A layer of silicon oxide 412 is formed over exterior surfaces 401a - 401f of structure 400. An oxide layer 416 is formed on the interior surface 409 of the through-opening 402, and

an oxide layer 418 is formed on the exterior surface, 411 of cylindrical region 406. The silicon disc 408 has been oxidized to form an oxide layer 414 in the through opening 402. Thickness of the disc 408 is typically selected so that it will be entirely converted to an oxide during the oxidation process.

[0055] The cylindrical region 406 is electrically isolated from surrounding region 404 by a combination of silicon oxide layers 416, 418, and 414, and by the air or vacuum space adjacent these oxide layers. Depending on the distance between these areas, the maximum breakdown voltage can be in the kilovolts range. The disk 408 can also act as a separation wall between two areas of structure 400 which are exposed to different pressures. For example an open space within area 410 may be at a given pressure while the open space within area 411 is under vacuum. It is understood that the shape of the isolation regions can be any shape and need not be cylindrical.

[0056] Figure 4C shows a schematic of the silicon structure in Figure 4B after that the structure has been lapped and polished and the oxide layer 412 present on the exterior wall surfaces 401e and 401f of structure 400 has been removed. It is understood that the layer 412 could be retained on any of the surfaces if desired. The space between the two oxide layers 416 and 418 may be filled with silicon oxide by CVD deposition if necessary, using techniques known in the art.

[0057] Figures 5A-5C show an alternative method of providing electrical isolation for a structure similar to the kind shown in Figures 4A-4C. Figure 5A shows a cylindrical silicon structure 500 including a top surface 501a, a bottom surface 501b and an outer surface 501c. The cylindrical silicon structure 500 also includes an internal silicon-containing conductive or semiconductive cylinder 508 and an external silicon-containing conductive or semiconductive cylinder 506. The internal cylinder 508 was

created by etching multiple open spaces 504 to form a cylinder shape within structure 500. Between these open spaces 504 are spokes 510 of the silicon-containing conductive or semiconductive material. In the present embodiment external cylinder 506, cylinder 508 and spokes 510 are silicon. The spokes 510 in this embodiment exhibit a thickness t_1 while the open spaces extend for a horizontal distance d_1. The relationship between t_1 and d_1 is such that $d_1 = 2 \times t_1$, so that upon oxidation of spokes 510, and the surfaces of spaces 504, spaces 504 will be filled with silicon oxide. The number of spokes and open spaces required for a given structure 500 can be calculated by one skilled in the art, depending on the amount of process time available for thermal oxidation and the time required under oxidation conditions to convert the silicon to silicon oxide. With respect to wet thermal oxidation, at about 1150° C, typically about 24 hours are required to oxidize a silicon spoke which is about 4 μm thick.

[0058] Figure 5B shows the same structure 500 after the exposed surfaces of the structure 500 have been oxidized. Oxide cylinder 516 formed from oxidized spokes 510 electrically isolates internal silicon cylinder 508 from external silicon cylinder 506. This embodiment of the invention allows cylindrical structure 500 to be etched all the way through in one direction, to produce internal silicon cylinder 508, and external silicon cylinder 506, with spokes 510 holding the internal silicon cylinder 508 in place. This provides the advantage that only one side of the cylindrical structure 500 has to be masked during the etch process and only a single etch step needs to be carried out.

[0059] The spoke thickness, t_1 and the distance d_1 may be selected such that the entire open space 504 shown in Figure 5A is not filled during the oxidation. In such cases, vacuum may be maintained in any remaining areas. Also, in such instances where thermal oxidation is impractical for filling the open space 504 the remaining open space

may be filled with CVD-deposited silicon oxide, if desired. Figure 5 C shows the schematic of the silicon structure in Figure 5B after the structure has been lapped and polished to remove the oxide layer, 512 from the top surface 501a and bottom surface 501b.

[0060] The above described preferred embodiments are not intended to limit the scope of the present invention, as one skilled in the art can, in view of the present disclosure expand such embodiments to correspond with the subject matter of the invention claimed below.